

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Kazuaki Goto) Confirmation No.: 3051
)
Serial No.	:	10/811,835)
) Examiner: Yelena Rossoshek
Filed	:	March 30, 2004)
) Art Unit: 2825
For	:	METHOD OF DESIGNING A CIRCUIT LAYOUT OF A SEMICONDUCTOR DEVICE)) Date: November 24, 2008

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants hereby request formal review of the May 22, 2008, final office action because the Examiner fails to identify the presence of essential elements required to establish a *prima facie* case with respect to novelty under 35 U.S.C. § 102(b).

This paper is being filed concurrently with a Notice of Appeal and the requisite fee, as required in the guidelines for the New Pre-Appeal Brief Conference Pilot Program published in the July 12, 2005, Official Gazette Notice.

Claims 1-15 currently are pending, with claims 6-9 withdrawn from consideration by the Examiner as being drawn to a non-elected invention. Thus, claims 1-5 and 10-15 have been examined, of which claims 1-3 and 10-13 are finally rejected and claims 4, 5, 14 and 15 objected to as being dependent upon a rejected independent claim, but including allowable subject matter.

Starting on page 2 of the Action, claims 1-3 and 10-13 are rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Solomon et al. (U.S. Patent No. 6,446,248). This rejection under Section 102 should be withdrawn because the Solomon et al. patent fails to

describe each and every feature recited in the pending independent claims 1 and 10, and hence also in claims depending from these independent claims.

Each of independent claims 1 and 10 is directed to a method of designing a circuit layout of a semiconductor integrated circuit. Claim 1 recites *inter alia* the process of providing a spare underground cell having no interconnect patterns and contacts. Independent claim 10 similarly includes a recitation of providing a plurality of spare underground cells having no interconnect patterns and contacts. In the final Office Action, the Examiner alleges Figure 3A and column 5, lines 10-16 of the Solomon et al. patent describe a base cell 245 having no contacts. It is respectfully submitted, however, that the high level diagram of Figure 3A does not constitute evidence that the transistors shown in schematic representations have no contacts, as claimed. Contrary to the Examiner's assertions, Figure 3B shows a more detailed physical layout diagram of the base cell 245 (see, column 5, lines 44-45), and the cell 245 clearly has contacts. More specifically, the description of Figure 3B in column 5, line 66 to column 6, line 11 explicitly mentions contacts, which are shown as the cross-hatched regions located on each transistor (see that the Figure 3B legend explicitly indicates these regions as "contacts").

For at least these reasons, the Solomon et al. patent does not describe all the claimed features of independent claims 1 and 10. Accordingly, the Section 102 rejection is in error and should be withdrawn.

Claims 2, 3 and 11-13 depend from one of independent claims 1 and 10, and are therefore also allowable at least for the above reasons, and further for the additional features recited.

In view of all of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and prompt notification of the same is earnestly sought.

Respectfully submitted,

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